TEXAS INSTRUMENTS

IEEE Std 1149.1 (JTAG) Testability

Primer

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Chapter 1
Introduction

Design for test (DFT), also known as *design for testability,* is a process that incorporates rules and techniques in the design of a product to make testing easier.

Structured design for test is a system methodology rather than a collection of discrete techniques. This methodology impacts all phases of a product's life, from device circuit design through field service. Design for test is used to manage complexity, minimize development time, and reduce manufacturing costs.

Testing has two major aspects: control and observation. To test any system it is necessary to put the system into a known state, supply known input data (test data), and observe the system to see if it performs as designed and manufactured. If control or observation cannot be carried out, there is no way to know empirically if the system performs as it should.

During the normal product development flow, testing (it may be known by different names) takes place at many points during the process. If testing is considered at the chip design level, its benefits can be used at all levels of electronic assembly, from chip through system level. See Figure 1-1.

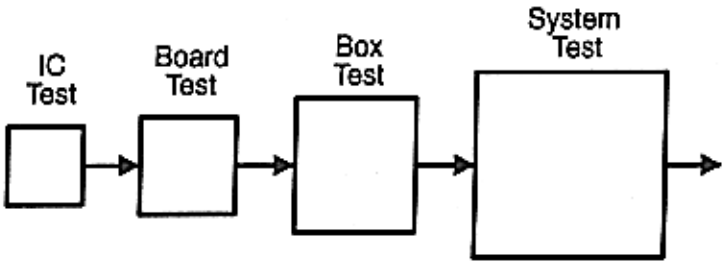

Figure 1-1. Chip Through System-Level Test

Designers usually test various functions to validate their design. Manufacturing and customer groups subject the design to an assortment of unique criteria to see if the concept works in practice. Is it manufacturable? Will it stand up to real-world operating conditions? Will repair be cost efficient? In addition to direct testability considerations, production managers want features designed into the product to help them minimize scrap and manufacturing costs. Good system-testability methodology provides an integrative function throughout the product development cycle and allows materials created during an early phase of development to be reused in later phases. Various chip designers have used this integration feature as a tool to help manage the development of complex products.

Testability provides companies with a firmer grasp on the economic and market-window constraints due to product development. One major workstation manufacturer claimed:

- Test program development would have been nearly impossible without scan techniques.
- Chip-level test development time fell from 1 man-year to about 20 hours.
- Board-level test development time fell from multiple man-years to about a week.
- Three months were cut off development time.

Overall Rationale for Design for Test

Manufacturers of state-of-the-art electronic products face a unique set of problems. Although modern circuit density, high device speed, surface-mount packaging, and complex board-interconnect technology have a positive influence on state-of-the-art electronic systems, these factors can adversely affect ability to verify correct design and operation. Increased complexity and lack of physical access to circuitry makes for costly and time-consuming testing using traditional test techniques.